

# A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by $N^2$

Xiang Gao, *Student Member, IEEE*, Eric A. M. Klumperink, *Senior Member, IEEE*, Mounir Bohsali, *Student Member, IEEE*, and Bram Nauta, *Fellow, IEEE*

**Abstract**—This paper presents a 2.2-GHz low jitter sub-sampling based PLL. It uses a phase-detector/charge-pump (PD/CP) that sub-samples the VCO output with the reference clock. In contrast to what happens in a classical PLL, the PD/CP noise is not multiplied by  $N^2$  in this sub-sampling PLL, resulting in a low noise contribution from the PD/CP. Moreover, no frequency divider is needed in the locked state and hence divider noise and power can be eliminated. An added frequency locked loop guarantees correct frequency locking without degrading jitter performance when in lock. The PLL is implemented in a standard 0.18- $\mu\text{m}$  CMOS process. It consumes 4.2 mA from a 1.8 V supply and occupies an active area of  $0.4 \times 0.45 \text{ mm}^2$ . With a frequency division ratio of 40, the in-band phase noise at 200 kHz offset is measured to be  $-126 \text{ dBc/Hz}$ . The rms PLL output jitter integrated from 10 kHz to 40 MHz is 0.15 ps.

**Index Terms**—Clock generation, clock multiplier, clocks, frequency multiplication, frequency synthesizer, jitter, loop noise, low jitter, low phase noise, low power, phase detector, phase locked loop (PLL), phase noise, sampling phase detector, sub-sampling phase detector, timing jitter.

## I. INTRODUCTION

A STABLE clock with low jitter and phase noise is a prerequisite for a variety of applications like high performance analog-to-digital converters, wireline and optical serial data communication links and radio transceivers. Of the many known PLL architectures [1], [2], the most widely-used “classical PLL” architecture [3]–[9] has a frequency divider divide-by- $N$ , a phase-detector(PD)/charge-pump(CP), a loop filter (LF) and a voltage controlled oscillator (VCO), see Fig. 1(a). A linear, phase domain model for the classical PLL together with various noise sources is shown in Fig. 1(b), with  $K_d$  the PD/CP detection gain,  $F_{LF}(s)$  the LF (trans-)impedance transfer function and  $K_{VCO}$  the VCO tuning gain. The PLL phase noise can be divided into two parts: 1) the VCO (and LF) noise which dominates out-of-band; 2) the loop noise (noise from the reference clock, PD/CP and divider) which dominates in-band as illustrated in Fig. 1(c). In an optimized PLL, the two types of noise contribute equally to the output jitter [2],

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X. Gao, E. A. M. Klumperink, and B. Nauta are with the IC-Design group, University of Twente, 7500 AE Enschede, The Netherlands (e-mail: x.gao@utwente.nl).

M. Bohsali is with National Semiconductor, Santa Clara, CA.

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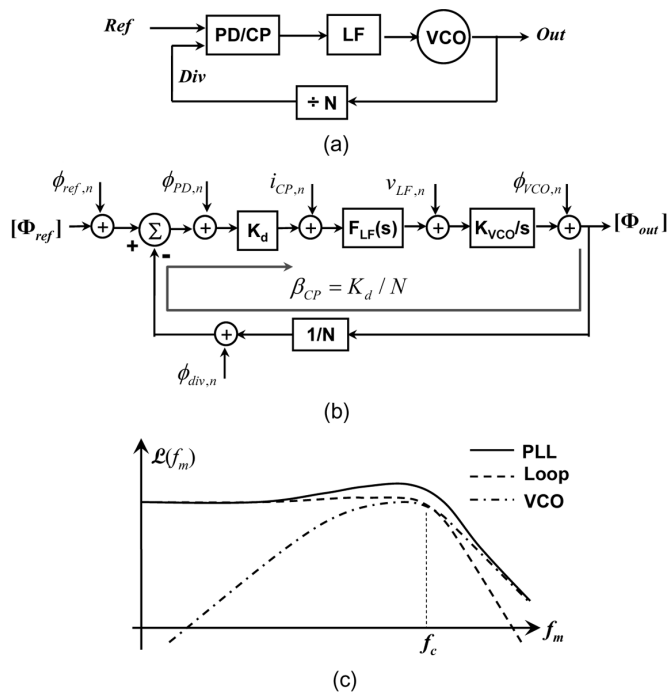


Fig. 1. Classical PLL (a) architecture, (b) phase domain model, (c) phase noise spectrum ( $1/f$  noise neglected).

[10] and thus are equally important. The VCO phase noise has been studied in literature and noise reduction techniques have been addressed, e.g., in [11]–[13]. The focus of this paper is on reducing the loop noise, i.e., the PLL in-band phase noise. In a classical PLL, the main loop noise sources are usually the PD/CP and the divider. Due to the existence of the divide-by- $N$  in the feedback path, the PD/CP and divider noise (in power) is multiplied by  $N^2$  when transferred to the PLL output.

Unlike the classical phase detectors, e.g., the well-known three-state phase frequency detector (PFD), a sampling or sample-and-hold PD [1], [14] can work without using a divider. Thus, divider noise and power dissipation can be eliminated. However, using a sampling PD has drawbacks like the need for a large filter capacitor due to its large detection gain and limited acquisition range [1], which have kept it from wide use in fully integrated PLLs. In this paper, we describe our proposed (sub-)sampling PLL architecture [16] which overcomes the aforementioned drawbacks. In addition to the elimination of divider noise, analysis shows that, in contrast to what happens in a classical PLL, the PD/CP noise is not multiplied by  $N^2$  in this PLL. As a result, the in-band phase noise is greatly

improved which leads to a PLL design with very low jitter as well as low power.

This paper is arranged as follows. Section II discusses and compares the CP noise contributions in a PLL using a classical three-state PFD/CP and a PLL using a sub-sampling PD/CP. Section III describes the complete sub-sampling PLL architecture and the design techniques used to overcome the sub-sampling PLL drawbacks. The circuit level design is described in Section IV and the experimental results are presented in Section V. Finally, Section VI draws conclusions.

## II. LOW NOISE PHASE DETECTION

In the following sections, we will discuss the PD/CP noise, with focus on the CP noise which often dominates. In order to calculate the CP noise contribution in a feedback system like a PLL, it is convenient to define a CP feedback gain  $\beta_{CP}$  as the gain from the PLL output to the CP output current. Using the phase domain model in Fig. 1(b), the close loop CP noise transfer function can be calculated as

$$\begin{aligned} H_{CP}(s) &= \frac{\phi_{out,n}}{i_{CP,n}} = \frac{1}{\beta_{CP}} \cdot \frac{\beta_{CP} \cdot F_{LF}(s) \cdot \frac{K_{VCO}}{s}}{1 + \beta_{CP} \cdot F_{LF}(s) \cdot \frac{K_{VCO}}{s}} \\ &= \frac{1}{\beta_{CP}} \cdot \frac{G(s)}{1 + G(s)} \end{aligned} \quad (1)$$

where  $G(s)$  is the PLL open loop transfer function.

Inside the PLL bandwidth,  $G(s) \gg 1$  and the PLL in-band phase noise contributed by the CP can be approximated as

$$\mathcal{L}_{in-band,CP} \approx \frac{1}{2} \cdot S_{i_{CP,n}} \cdot |H_{CP}(s)|^2 \approx \frac{S_{i_{CP,n}}}{2\beta_{CP}^2} \quad (2)$$

where the phase noise is expressed with the often used single sideband noise power to carrier power ratio  $\mathcal{L}$  and  $S_{i_{CP,n}}$  is the power spectral density of the CP current noise.

Equation (2) indicates that the CP noise is suppressed by  $(\beta_{CP})^2$  when transferred to the PLL output. A larger  $\beta_{CP}$  is thus desired as it provides more suppression for the CP noise.

### A. Classical Three-State PFD/CP

For PLL designs, the three-state PFD/CP as shown in Fig. 2 is often used. The VCO output is firstly divided down so that the divider output Div has the same frequency as the reference clock Ref. The timing/phase of Div and Ref are then compared and the CP outputs a current pulse with width equal to the amount of timing/phase error. The CP feedback gain of the classical three-state PFD/CP can be calculated as

$$\begin{aligned} \beta_{CP,PFD} &= \frac{\Delta \overline{i_{CP}}}{\Delta \phi_{VCO}} = \frac{I_{CP} \cdot \left( \frac{\Delta \phi_{div}}{2\pi} \right)}{\Delta \phi_{VCO}} = \frac{I_{CP}}{2\pi} \cdot \frac{1}{N} \\ &= K_d \cdot \frac{1}{N} \end{aligned} \quad (3)$$

where  $I_{CP}$  is the bias current of the CP current sources,  $\overline{i_{CP}}$  is the mean CP output current,  $\Delta \phi_{VCO}$  and  $\Delta \phi_{div}$  are respectively the VCO and divider phase error. Equation (3) indicates that  $\beta_{CP,PFD}$  is reduced by the frequency division ratio  $N$ . That is the reason why the CP noise power is multiplied by  $N^2$  as according to (2) the CP noise contribution is inversely proportional to  $(\beta_{CP})^2$ .

The reduction of  $\beta_{CP,PFD}$  by the division ratio is perhaps easier understood in the time domain where the VCO timing error is directly transferred to the divider output without scaling. When a timing error  $\Delta t$  between the VCO/Div and Ref is detected, the CP will output a current pulse with width  $\Delta t$ . The mean CP output current is then  $I_{CP} \cdot \Delta t / T_{ref}$  with  $T_{ref}$  the period of Ref. If we increase  $N$  while keeping  $f_{VCO}$  the same,  $f_{ref}$  becomes lower and  $T_{ref}$  becomes larger. On the other hand, the width of the CP output current pulse remains the same for the same amount of VCO/Div timing error. Consequently, the mean CP output current becomes smaller due to the larger  $T_{ref}$ , corresponding to a lower  $\beta_{CP,PFD}$ .

It is possible to physically eliminate the divider (and its noise contribution) and design a three-state PFD/CP based divider-less PLL as proposed in [17], where the PFD compares the phase of the VCO and Ref at every rising edge of Ref for only a small time window (aperture). However, since the phase detection mechanism remains the same,  $\beta_{CP,PFD}$  remains proportional to  $\Delta t / T_{ref}$  meaning that it is still reduced by  $N$  and the CP noise is still multiplied by  $N^2$ .

In steady state, a CP driven by a PFD is switched on only for  $\tau_{PFD}$  in each period  $T_{ref}$ . Assuming that the noise of the CP UP/DN current source is dominated by a single MOS transistor with transconductance  $g_m$ , the power spectral density of the (thermal) noise generated by the CP can be estimated as [10]:

$$S_{i_{CP,n,PFD}} = 8kT\gamma \cdot g_m \cdot \frac{\tau_{PFD}}{T_{ref}} \quad (4)$$

where  $\gamma$  is a noise model parameter of the MOS transistor typically in the range of 2/3 to 1.5.

### B. Proposed Sub-Sampling PD/CP

The sampling based PD has been known for years [14]. Fig. 3 shows its conceptual diagram and timing diagram. The VCO output, a sine wave with amplitude  $A_{VCO}$  and DC voltage  $V_{DC}$ , is sampled by a reference clock Ref. When the VCO and Ref are phase aligned and their frequency ratio  $N$  is an integer, the sampled voltage  $V_{sam}$  has a constant value equal to  $V_{DC}$ . When there is phase error between the VCO and Ref,  $V_{sam}$  will deviate from  $V_{DC}$ . The voltage difference between  $V_{sam}$  and  $V_{DC}$  represents the amount of phase error as shown in Fig. 3(b). Note that this PD works without using a divider as soon as the ratio  $f_{VCO}/f_{ref}$  is an integer, which is an often mentioned reason to use it. However, we will show below that a (sub-)sampling PD can also bring a significant phase noise benefit.

In a sampling PD, the timing/phase error is converted into voltage error. Since the high frequency VCO has a high slew rate:  $SR_{VCO} = A_{VCO} \cdot 2\pi f_{VCO}$ , a high detection gain can be expected. Fig. 4(a) shows the first step toward our sub-sampling PD/CP (SSPD/CP) proposal. The name sub-sampling is used to stress that the high frequency VCO is sampled by a low frequency Ref. In order to process  $V_{sam}$  via the traditional current driven loop-filter, a transconductor converts voltage  $V_{sam}$  into current  $g_m V_{sam}$ , acting as UP current source. The DN current source is controlled by  $V_{DC}$ , the expected VCO voltage when sampled at the crossing moment. Thus, in contrast to a traditional CP, the output current is not proportional to  $\Delta t / T_{ref}$ , but rather amplitude controlled by the difference of  $V_{sam}$  and  $V_{DC}$ , which is proportional to  $\Delta t / SR_{VCO}$ . The transfer characteristic of the SSPD/CP has the same shape as the VCO waveform, as

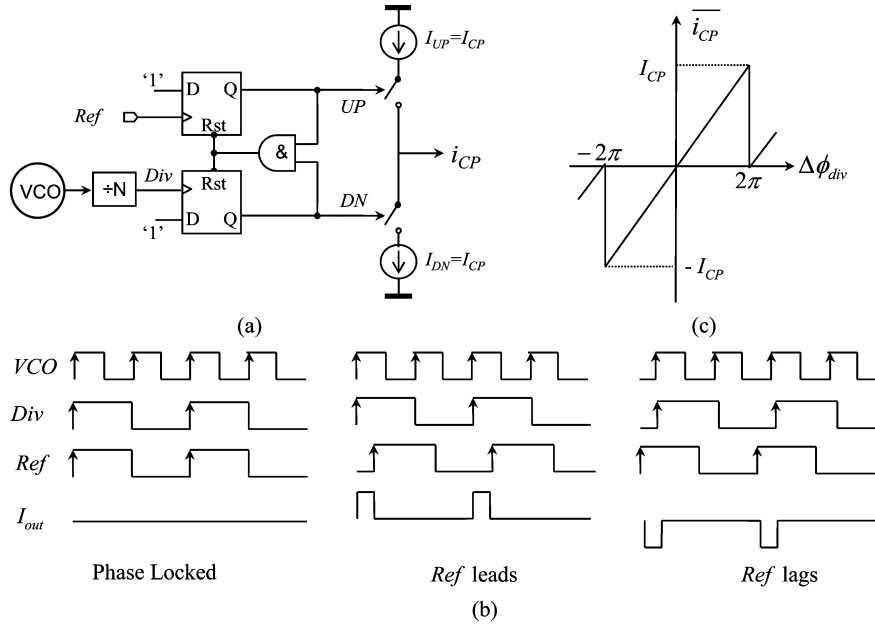


Fig. 2. Three-state PFD/CP: (a) schematic, (b) timing diagram, (c) characteristic.

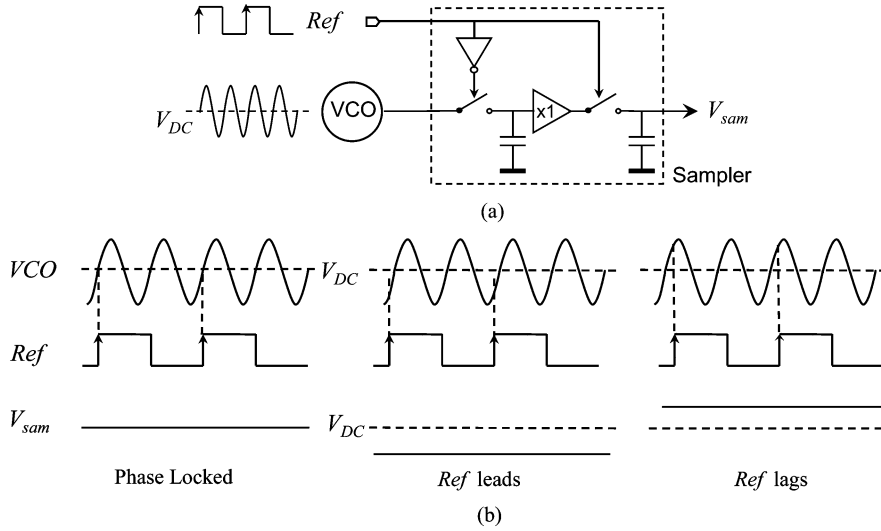


Fig. 3. Sampling based PD: (a) conceptual diagram; (b) timing diagram.

shown in Fig. 4(b). The ideal locking point is the crossing moment of the sine wave (corresponding to  $V_{sam} = V_{DC}$ ) where it is most linear. The sinusoidal characteristic of the SSPD is similar to that of a mixer based phase detector. However, the SSPD is not sensitive to the duty cycle or shape of the sampling reference clock as it only takes one sample per period instead of processing the whole VCO waveform.

The architecture of a PLL utilizing the SSPD/CP, which we call a sub-sampling PLL (SSPLL), is shown in Fig. 5(a). In the steady state, the VCO phase error is small and the CP feedback gain of the SSPLL can be calculated as

$$\beta_{CP,SS} = K_d = \frac{\Delta \overline{i_{CP}}}{\Delta \phi_{VCO}} = \frac{A_{VCO} \sin(\Delta \phi_{VCO}) \cdot g_m}{\Delta \phi_{VCO}} \approx A_{VCO} \cdot g_m. \quad (5)$$

We see that there is no  $N$  in (5), which means that  $\beta_{CP,SS}$  is not related to  $N$ . Consequently, the CP noise of the SSPLL is not multiplied by  $N^2$  when transferred to the output.

Assuming that the CP current source is implemented with a single square-law MOS transistor, (5) can be rewritten as

$$\beta_{CP,SS} = K_d = A_{VCO} \cdot \frac{2I_{CP}}{V_{gs,eff}} \quad (6)$$

where  $V_{gs,eff}$  is the effective gate-source voltage of the MOS transistor and  $2I_{CP}/V_{gs,eff}$  represents  $g_m$ .

Unlike the three-state PFD/CP, the two current sources in the SSPD/CP are always on. The equivalent CP (thermal) noise current can be estimated as

$$S_{i_{CP,n,SS}} = 8kT\gamma \cdot g_m. \quad (7)$$

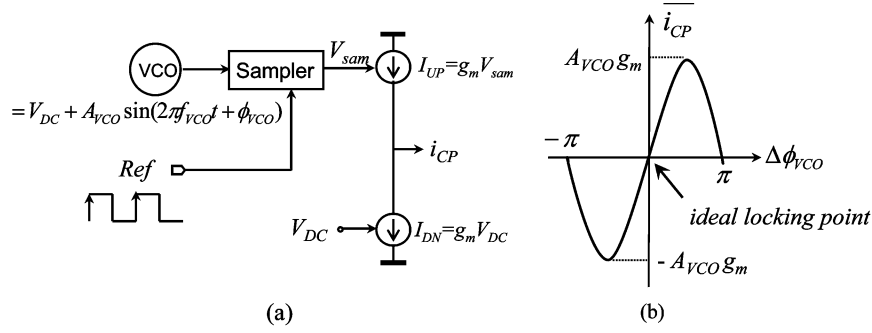


Fig. 4. Conceptual schematic and characteristic of a sub-sampling based PD/CP.

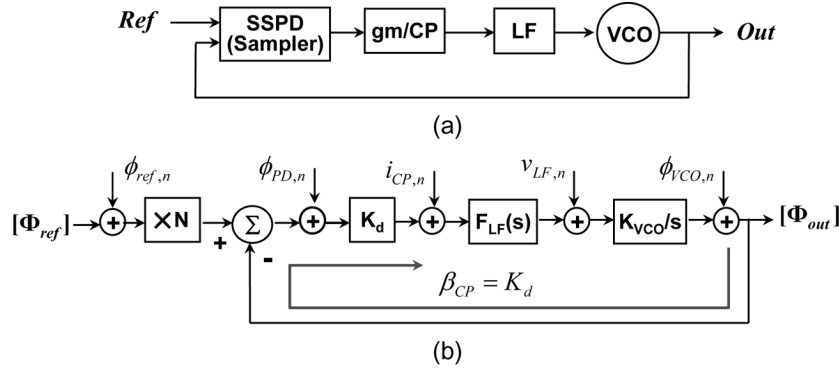


Fig. 5. Sub-sampling PLL: (a) architecture, (b) phase domain model.

### C. CP Noise Comparison

In this section, we compare the CP noise contribution of a classical PLL using the three-state PFD/CP and a SSPLL using the SSPD/CP. In both PLLs, the CP noise contribution can be reduced by increasing the CP bias current  $I_{CP}$ . For a fair comparison, we assume the two CPs use equal  $I_{CP}$ .

The CP feedback gain of the classical PLL and the SSPLL can be compared using (3) and (6) as

$$\frac{\beta_{CP,SS}}{\beta_{CP,PFD}} = 4\pi \cdot N \cdot \frac{A_{VCO}}{V_{gs,eff}}. \quad (8)$$

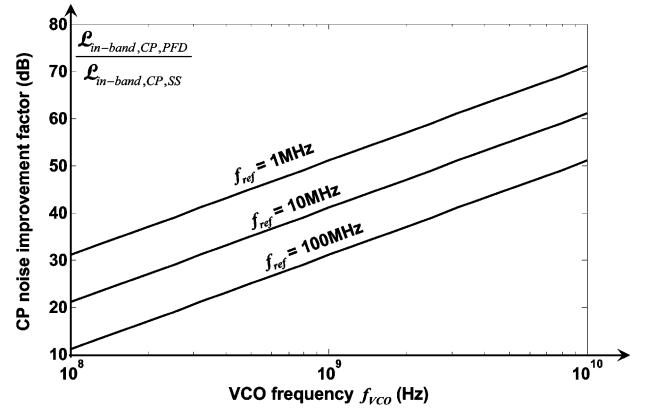
It is easy to see that (8) is much larger than 1 as  $4\pi \gg 1$ ,  $N \geq 1$  (most often  $\gg 1$ ) and usually  $A_{VCO} > V_{gs,eff}$ . Thus, the SSPLL has a *much larger*  $\beta_{CP}$  than the classical PLL, and thus has much more suppression for the CP noise.

On the other hand, the CP in the SSPLL is always on and continuously injects noise to the loop filter, while the CP in the classical PLL only injects noise for a fraction of time  $\tau_{PFD}$  during each  $T_{ref}$ . Effectively, the CP in the classical PLL generates  $\tau_{PFD}/T_{ref}$  times less (thermal) noise than the CP in the SSPLL:

$$\frac{S_{i_{CP,n,PFD}}}{S_{i_{CP,n,SS}}} = \frac{\tau_{PFD}}{T_{ref}}. \quad (9)$$

Overall, the in-band phase noise due to the CP of the two PLLs can be compared using (2), (8) and (9) as

$$\begin{aligned} \frac{\mathcal{L}_{in-band,CP,PFD}}{\mathcal{L}_{in-band}} &= \left(4\pi \cdot N \cdot \frac{A_{VCO}}{V_{gs,eff}}\right)^2 \cdot \left(\frac{\tau_{PFD}}{T_{ref}}\right) \\ &= \left(4\pi \cdot \frac{A_{VCO}}{V_{gs,eff}} \cdot \sqrt{\tau_{PFD}}\right)^2 \cdot \left(\frac{f_{VCO}^2}{f_{ref}}\right). \quad (10) \end{aligned}$$

Fig. 6. Theoretical CP noise improvement factor (10) as a function of the VCO frequency for various reference frequencies, assuming  $A_{VCO} = 0.4$  V,  $V_{gs,eff} = 0.2$  V and  $\tau_{PFD} = 200$  ps.

The value of (10) indicates the amount of CP noise reduction we can achieve by using a SSPLL instead of a classical PLL. Assuming  $A_{VCO} = 0.4$  V,  $V_{gs,eff} = 0.2$  V and  $\tau_{PFD} = 200$  ps, the ratio in (10) is plotted in Fig. 6 for  $f_{ref}$  ranging from 1 MHz to 100 MHz and  $f_{VCO}$  ranging from 100 MHz to 10 GHz. We see that the SSPLL has orders of magnitude less CP contributed in-band phase noise than the classical PLL. The advantage of the SSPLL is larger when a higher  $f_{VCO}$  or a lower  $f_{ref}$  are used.

### III. SUB-SAMPLING PLL

Although the sampling PD has been existing for years, its potential of achieving very low in-band phase noise is not fully appreciated to the best of our knowledge. It also has drawbacks like difficulty of integration (large filter capacitor needed) and limited frequency acquisition range [1], which have kept it from wide use in full integrated PLLs. The sampling PD has been

used in a MMIC PLL [15] and a DLL [22]. However, both of them use off-chip loop filters. The CDR in [21] also uses a sampling PD but the division ratio is one. To the best of the authors' knowledge, our design [16] is the first fully integrated sub-sampling PD based PLL. In the following sub-sections, we will build a phase domain model for the SSPLL and compare its phase noise with the classical PLL. We will also discuss SSPLL drawbacks and propose design techniques [16] to overcome them.

### A. Modeling and Noise Analysis

A linear phase-domain model for the SSPLL is shown in Fig. 5(b). Here we model the SSPLL as a time continuous system, which is valid as soon as the PLL bandwidth is an order of magnitude smaller than  $f_{\text{ref}}$  [18]. In case the bandwidth is higher, the sampling effects will affect loop stability. They can be modeled using the method in [1] and can be added into Fig. 5(b).

Unlike the classical PLL, there is no divide-by- $N$  in the feedback path in the SSPLL model. Instead, a virtual frequency multiplier " $\times N$ " is added to the reference clock path. This (physically non-existing) multiplier originates from the sub-sampling process. When the high frequency VCO is sub-sampled by the low frequency Ref, the baseband alias falling in the loop filter band has a frequency of:

$$f_{\text{alias}} = f_{\text{VCO}} - N \cdot f_{\text{ref}}. \quad (11)$$

Therefore, the sub-sampling process works as if the VCO is sampled by a signal with frequency  $N$  times higher than Ref. In other words, the frequency and thus phase of Ref is virtually multiplied by  $N$ . Viewed in another way, the sampler output voltage is proportional to the timing error between the VCO and Ref. However, a given timing error corresponds to  $N$  times more phase error if we refer it to the VCO instead of Ref since  $f_{\text{VCO}} = N \cdot f_{\text{ref}}$ . As the phase of the VCO is subtracted at the phase comparison point, a multiplication  $\times N$  of the phase of Ref before this subtraction point is incorporated in the model.

Using this phase domain model for noise analysis, we see that the reference clock phase noise is still multiplied by  $N^2$  when transferred to the output, same as in a classical PLL. However, due to the absence of the divide-by- $N$  in the feedback path<sup>1</sup> both the CP and PD noise is not multiplied by  $N^2$ . Moreover, the SSPLL does not need a divider in the locked state, thus the divider noise is eliminated. Therefore, we can expect the SSPLL to achieve a much lower in-band phase noise than the classical PLL. The CP noise analysis was already done in Section II (Fig. 6). The noise contribution of the SSPD can be calculated by relating the voltage noise at the SSPD output  $\overline{v_{\text{SSPD},n}^2}$  and the corresponding VCO phase error in steady state:

$$\overline{v_{\text{SSPD},n}^2} = \frac{kT}{C_{\text{sam}}} \approx (A_{\text{VCO}} \cdot \Delta\phi_{\text{VCO,SSPD}})^2 \quad (12)$$

where  $C_{\text{sam}}$  is the sampling capacitor value.

Assuming white noise and using the fact that the SSPD noise is band-limited by  $f_{\text{ref}}/2$  due to sampling, the PLL in-band phase noise due to the SSPD can be calculated as

$$2\mathcal{L}_{\text{in-band,SSPD}} \times \frac{f_{\text{ref}}}{2} = (\Delta\phi_{\text{VCO,SSPD}})^2. \quad (13)$$

<sup>1</sup>Compared with the divider-less PLL in [17], the SSPLL does not only eliminate the physical divider, but also eliminate the divider in the phase domain model. In this sense it is a truly divider-less PLL.

Using (12) and (13), we get:

$$\mathcal{L}_{\text{in-band,SSPD}} = \frac{kT}{C_{\text{sam}} \cdot A_{\text{VCO}}^2 \cdot f_{\text{ref}}}. \quad (14)$$

We see that the SSPD noise is indeed not multiplied by  $N^2$ . Because of that, its contribution to the overall in-band phase noise can be small without using a big  $C_{\text{sam}}$ . As a numerical example, with  $f_{\text{ref}} = 55$  MHz and  $A_{\text{VCO}} = 0.4$  V, a 10 fF  $C_{\text{sam}}$  is sufficient to bring  $\mathcal{L}_{\text{in-band,SSPD}}$  to be as low as  $-133$  dBc/Hz.

### B. Chip Area Considerations

In a charge pump PLL, the most common implementation of the loop filter is a passive  $RC$  filter where a resistor  $R_1$  is in series with a capacitor  $C_1$ . A second capacitor  $C_2$  is often added in parallel to reduce the voltage ripple. In order to integrate the loop filter on chip, the value of  $C_1$  and  $C_2$  should not be too large. In the following discussions we will neglect  $C_2$  since it is much smaller than  $C_1$  and is not the major concern.

Substituting the loop filter transfer function  $F_{\text{LF}} = R_1 + 1/sC_1$  into the PLL phase domain model in Fig. 5(b), the PLL open loop bandwidth  $f_c$  and the frequency of the loop gain zero  $f_{\text{zero}}$  can be expressed as

$$f_c = \frac{\omega_c}{2\pi} \approx \frac{\beta_{\text{CP}} \cdot R_1 \cdot K_{\text{VCO}}}{2\pi} \quad (15)$$

$$f_{\text{zero}} = \frac{1}{2\pi \cdot R_1 C_1}. \quad (16)$$

Combining (15) and (16), we get:

$$C_1 = \left\{ \frac{K_{\text{VCO}}}{4\pi^2} \cdot \frac{f_c}{f_{\text{zero}}} \right\} \cdot \frac{\beta_{\text{CP}}}{f_c^2}. \quad (17)$$

In (17),  $K_{\text{VCO}}$  is related to the VCO analog tuning range requirement and  $f_c/f_{\text{zero}}$  is related to the phase margin requirement. Once they are specified, the bracketed part is a constant. The value of  $C_1$  is thus proportional to  $\beta_{\text{CP}}$  and inversely proportional to the square of  $f_c$ .

In order to achieve low output jitter, the PLL bandwidth  $f_c$  needs to be carefully chosen. The optimal bandwidth  $f_{c,\text{opt}}$  for minimum jitter is roughly where the spectrum of the VCO and the loop noise intersects [2], [10]. For lower loop noise,  $f_{c,\text{opt}}$  is thus higher, requiring a smaller  $C_1$ . When the loop noise is dominated by the CP noise, having a larger  $\beta_{\text{CP}}$  reduces the loop noise and increases  $f_{c,\text{opt}}$  as shown in Fig. 7(a). However, when the CP noise becomes negligible and other loop components' noise start dominating the loop noise, having a further larger  $\beta_{\text{CP}}$  still reduces the CP noise but will hardly reduce the overall loop noise as shown in Fig. 7(b). In the latter case, increasing  $\beta_{\text{CP}}$  further can not increase  $f_{c,\text{opt}}$ , but does require a larger  $C_1$  to stabilize the PLL. Such an "unnecessarily high"  $\beta_{\text{CP}}$  will thus make full integration difficult. Fig. 6 shows that the SSPLL reduces the CP noise contribution so much that it easily becomes negligible. Therefore,  $\beta_{\text{CP,SS}}$  easily enters the "unnecessarily high" region and it is actually desired to reduce  $\beta_{\text{CP,SS}}$  in order to reduce filter capacitor area.

### C. SSPD/CP With Gain Control

Fig. 8 shows the proposed SSPD/CP with gain reduction. Instead of leaving the CP always on, two switches and a block called "Pulser" are added. Also, antiphase VCO outputs and differential sampling are used. The locking point is then the crossing moment of the differential VCO outputs with no need

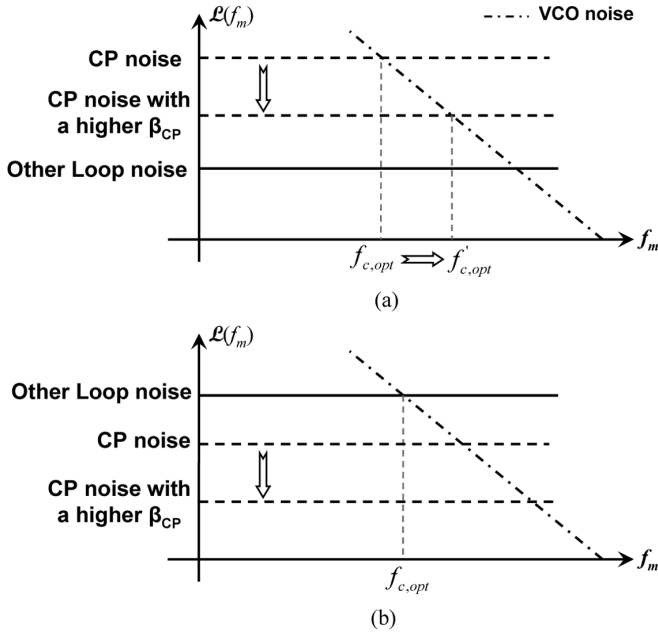


Fig. 7. Relation between  $\beta_{CP}$  and  $f_{c,opt}$  for dominant and non-dominant CP noise (conceptual).

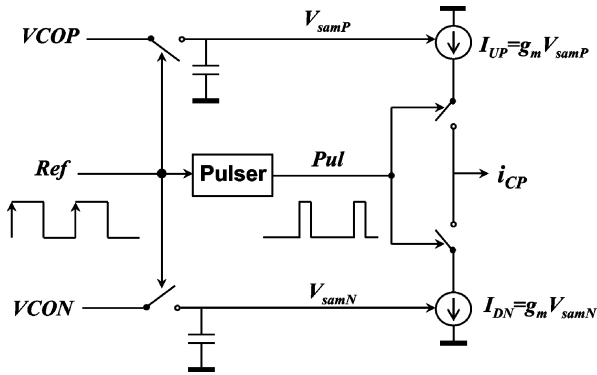


Fig. 8. Schematic of proposed sub-sampling PD/CP with pulsewidth gain reduction.

for a reference voltage  $V_{DC}$  as in Fig. 4. Using differential sampling also alleviates charge injection and charge sharing issues and helps to reject supply noise.

The Pulser generates a pulse with width  $\tau_{pul}$  and simultaneously switches on the UP and DN current sources for a fraction of time  $\tau_{pul}$  in each Ref period  $T_{ref}$ . In this way, the mean CP output current and thus  $\beta_{CP,SS}$  is reduced by  $\tau_{pul}/T_{ref}$ :

$$\beta_{CP,SS} = 2A_{VCO} \cdot g_m \cdot \frac{\tau_{pul}}{T_{ref}}. \quad (18)$$

The additional factor of 2 in (18) compared with (5) is due to the use of differential sampling. On the other hand, switching on the current sources only for a fraction of time also reduces CP noise:

$$S_{i_{CP,n,SS}} = 8kT\gamma \cdot g_m \cdot \frac{\tau_{pul}}{T_{ref}}. \quad (19)$$

Since the reduction of the CP noise suppression factor  $(\beta_{CP,SS})^2$  is stronger than the reduction of the CP noise

$S_{i_{CP,n,SS}}$ , the overall effect is that the in-band phase noise due to CP increases with  $T_{ref}/\tau_{pul}$ :

$$\mathcal{L}_{in-band,CP,SS} \approx \frac{S_{i_{CP,n,SS}}}{2\beta_{CP,SS}^2} = \frac{kT\gamma}{A_{VCO}^2 \cdot g_m} \cdot \frac{T_{ref}}{\tau_{pul}}. \quad (20)$$

By a careful choice of  $\tau_{pul}/T_{ref}$ , the value of  $\beta_{CP,SS}$  will not be ‘‘unnecessarily high’’ but still high enough to keep the CP a negligible source of the loop noise. In this way, the low noise feature of the SSPD/CP can be explored without paying unnecessary filter capacitor area.

Apart from gain reduction, the Pulser also has a second role. In a normal sampler implementation, two non-overlapping track and hold circuits are needed in order to make the sampled voltage a constant DC value as shown in Fig. 3. By designing the Pulser such that its output has no overlap with the sampling clock Ref, only one track and hold circuit is needed to implement the sampler; see Fig. 8. In other words, adding the Pulser and the two switches eliminates the need for the second track and hold circuit.

The proposed CP in Fig. 8 may at first sight look similar to the conventional CP in Fig. 2. However, a key difference is that in the proposed CP the current source amplitude is controlled by the SSPD while in the conventional CP the current source switch-on time is controlled by the PFD. Combined with the SSPD, the proposed CP has the unique feature that the CP noise is not multiplied by  $N^2$ .

#### D. Frequency Locking

Due to its sinusoidal characteristic, the SSPD has limited frequency acquisition range similar to the case of the mixer based PD. Moreover, the sub-sampling process can not distinguish between  $N \cdot f_{ref}$  and other harmonics of  $f_{ref}$  and thus the SSPLL may false lock to an unwanted division ratio. Therefore, measures are needed to guarantee frequency lock.

Fig. 9 shows the top-level block diagram of the proposed SSPLL. The core loop consists of a SSPD/CP, a Pulser, a passive loop filter and a VCO. In order to ensure correct locking of the PLL, a frequency-locked loop (FLL) is added. The FLL consists of a divide-by- $N$  and a three-state PFD/CP as in a classical PLL, except that a dedicated dead zone (DZ) is inserted between the PFD and CP. The intended PLL action is as follows. When  $f_{VCO}$  is much different from  $N \cdot f_{ref}$ , the phase/frequency error between VCO and Ref is large and falls outside of the FLL DZ. The FLL has a larger gain than the core loop, dominates the loop control and brings down  $|f_{VCO} - N \cdot f_{ref}|$ . When it is close to locking, the phase error between VCO and Ref is small and falls inside the FLL DZ. The output current of the CP in the FLL will then be zero. The loop settles with a time constant determined by the core loop. The FLL and the divide-by- $N$  then have no influence on the core loop and do not degenerate the PLL jitter performance. In order to realize the aforementioned functions, the width of the DZ is set larger than the expected jitter at the VCO output in the locked state. The bias current for the FLL CP should be set large enough so that the FLL dominates the loop control outside the DZ. After locking is achieved, the FLL can also be disabled to save power.

## IV. DESIGN AND IMPLEMENTATION

### A. Phase Detector and Charge Pump

Fig. 10 shows the SSPD/CP schematic. The differential sampler is implemented simply with two NMOS transistors and two

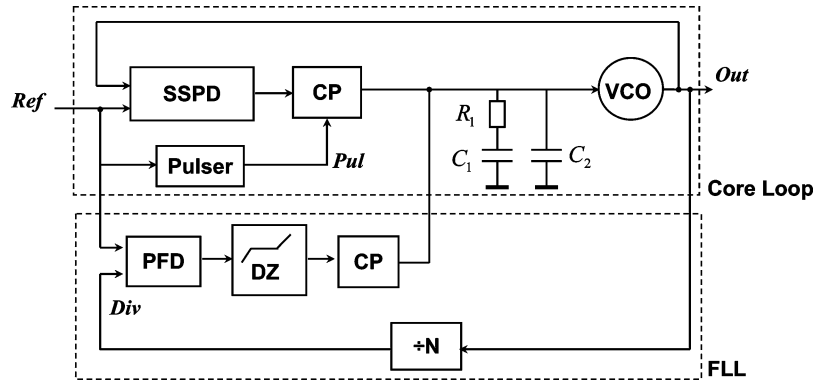


Fig. 9. Block diagram of the proposed SSPLL.

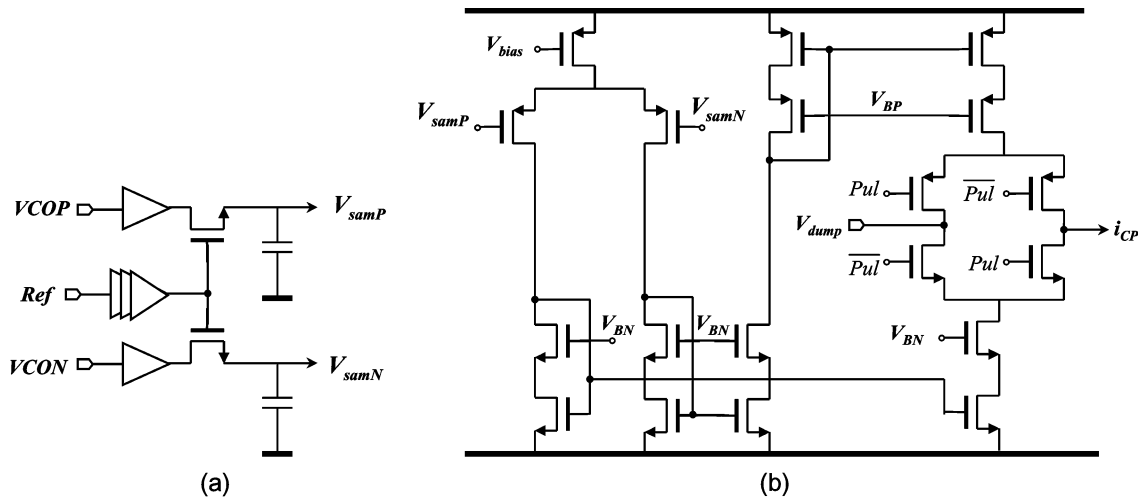


Fig. 10. Schematic of (a) sub-sampling phase detector, and (b) charge pump.

poly-poly capacitors. Two source follower buffers isolate the sampler from the VCO. Since the buffers also add noise, the SSPD noise contribution is larger than the one calculated in (14). The value of the sampling capacitor is chosen to be 60 fF so that the noise from the sampler and its buffer contributes to less than 20% of the overall loop noise. The CP is realized with a differential pair which converts voltage into current and cascode current mirrors which diverts the current into the loop filter. When the Pulser output  $Pul$  is high, the CP UP and DN current sources are connected and inject currents into the loop filter. When  $Pul$  is low,  $\overline{Pul}$  is high. The current sources are steered away to a voltage  $V_{dump} = V_{DD}/2$  instead of switched off to alleviate the charge sharing between the loop filter and the current sources. In the locked state, the VCO phase error is small and the SSPD/CP characteristic is fairly linear.

Since the crystal oscillator output is a low slew-rate sine-wave, an inverter chain is used as Ref buffer to convert it into a steep square wave. To achieve low PLL in-band phase noise, the Ref noise is critical as it will be multiplied by  $N^2$  when transferred to the output. Since a high quality crystal oscillator has low phase noise, the buffer is the major source of the Ref noise. The inverter chain especially the first inverter in the chain is sized large to reduce noise, at the expense of power consumption. Interestingly, we observed that the SSPLL has such a low PD/CP noise (and no divider noise) that the Ref buffer becomes the dominant source of the in-band phase noise as well as the dominant source of the power consumption. Simulation shows

that it consumes 60% of the total loop power while contributing 50% of the in-band phase noise. We will come back to this in Section V.

The Pulser is implemented using a delay cell and a few logic gates as shown in Fig. 11(a). Fig. 11(b) illustrates the timing of the signals. The width of  $Pul$  is determined by the amount of delay  $\tau_{pul}$  of the delay cell which has a nominal value of 1.5 ns. The delay cell is realized with two inverters as shown in Fig. 11(c), where the charging and discharging currents of the output capacitance in the first inverter are controlled by  $V_{tune}$ . Therefore,  $\tau_{pul}$  can be controlled by  $V_{tune}$ . Since the sampling PLL loop gain is proportional to  $\tau_{pul}$  as shown in (18), the PLL loop bandwidth can be tuned by tuning  $V_{tune}$ . Note that this bandwidth tuning is done without affecting the operation point of the rest of the circuits. For experimental purposes,  $V_{tune}$  is fed from off-chip.

### B. Three-State PFD/CP With Dead Zone

The schematic of the three-state PFD/CP with dead zone is shown in Fig. 12(a). In addition to the conventional three-state PFD/CP, two D-flip-flops (DFFs) are inserted which resample the generated UP and DN pulses. Unlike the DFFs in the three-state PFD, the two added DFFs are triggered by the falling edges, which are  $T_{ref}/2$  delayed from the rising edges if the clock duty cycle is 50%. In this way, any UP and DN pulses with width smaller than  $T_{ref}/2$  will be “filtered” out, creating a timing dead zone of  $\pm T_{ref}/2$ . Fig. 12(b) shows one

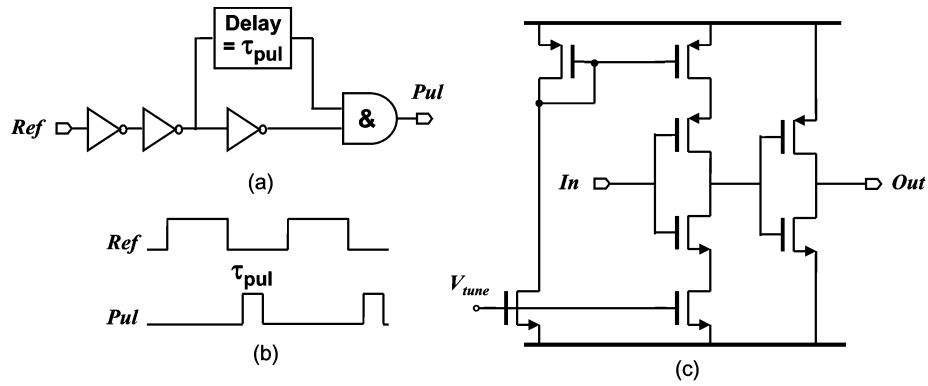


Fig. 11. Pulsar: (a) block diagram, (b) timing diagram, (c) tunable delay cell.

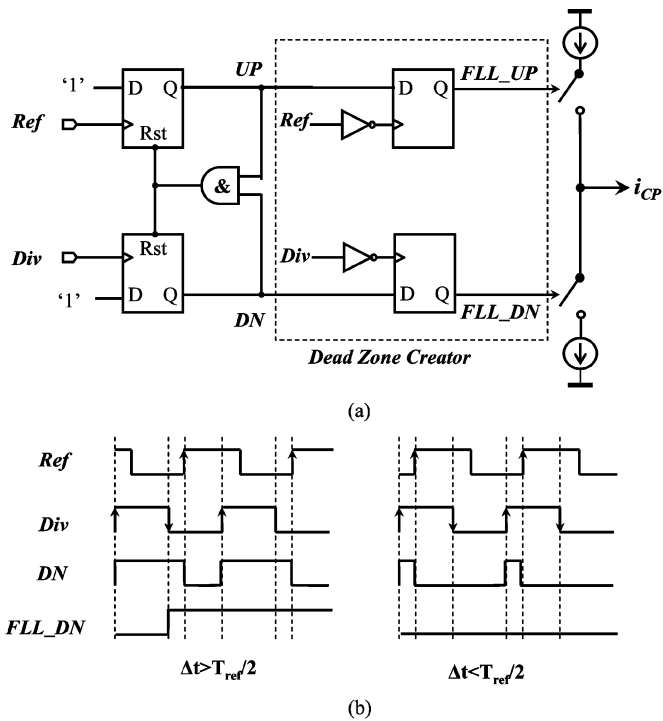


Fig. 12. Three-state PFD/CP with dead zone: (a) schematic, (b) example timing diagram when Ref lags.

example timing diagram when Ref lags illustrating no activity in the right case.

### C. VCO and Output Buffer

The LC-VCO used in this design is a (NMOS) current biased one with double switch pair. The quality factor of the inductor is approximately 5. The VCO has a tuning gain of 50 MHz/V. To increase the frequency tuning range, digital tuning by means of switching on/off MOS capacitors can easily be applied. The output buffer for measurements consists of a tapered multi-stage CML inverter chain. Each stage has three times the dimensions and one-third the resistance value of its predecessor. The final stage has 50  $\Omega$  on-chip termination resistors.

## V. EXPERIMENTAL RESULTS

To verify the ideas presented and demonstrate the low loop noise perspective, a prototype chip was designed and fabricated in a standard 0.18- $\mu\text{m}$  CMOS process. Fig. 13 shows

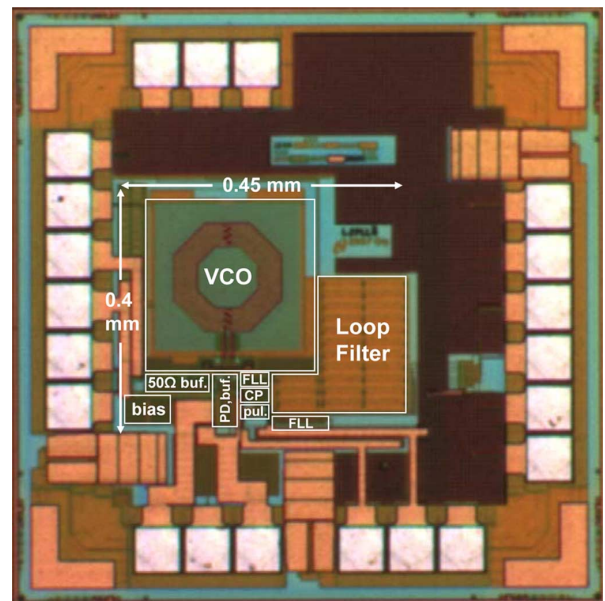


Fig. 13. Chip microphotograph.

a die micrograph. The total chip area including the pads is  $0.8 \times 0.8 \text{ mm}^2$ , while the active area is  $0.4 \times 0.45 \text{ mm}^2$  and is dominated by the LC VCO. Thanks to the use of the pulsewidth gain reduction in the SSPD/CP, the loop filter does not require large capacitors and is fully integrated. Aiming at a 60 degree phase margin, the largest filter capacitor  $C_1$  has a value of 90 pF. The IC was tested in a 24-pin Quad LLP package. Excluding the 50  $\Omega$  CML buffer for measurements, the PLL core (including the Ref buffer) consumes 4.2 mA from a 1.8 V supply. The VCO dissipates 1 mA, the Ref buffer 1.9 mA, and the rest circuits 1.3 mA. The FLL consumes 0.8 mA and is disabled after locking is achieved to save power.

The reference clock is derived from an off-chip high quality 55.25 MHz SC Sprinter crystal oscillator from Wenzel Associates. The crystal oscillator output passes an off-chip attenuator before it is fed into the chip; such that the signal arriving on-chip has 1.8  $V_{p-p}$  amplitude fitting to the 1.8 V supply. Fig. 14 shows the phase noise spectrum of the 2.21 GHz PLL output measured from an Agilent E5501B phase noise measurement setup. The in-band phase noise is  $-126 \text{ dBc/Hz}$  at 200 kHz offset and out-of-band phase noise is  $-141 \text{ dBc/Hz}$  at 20 MHz offset.



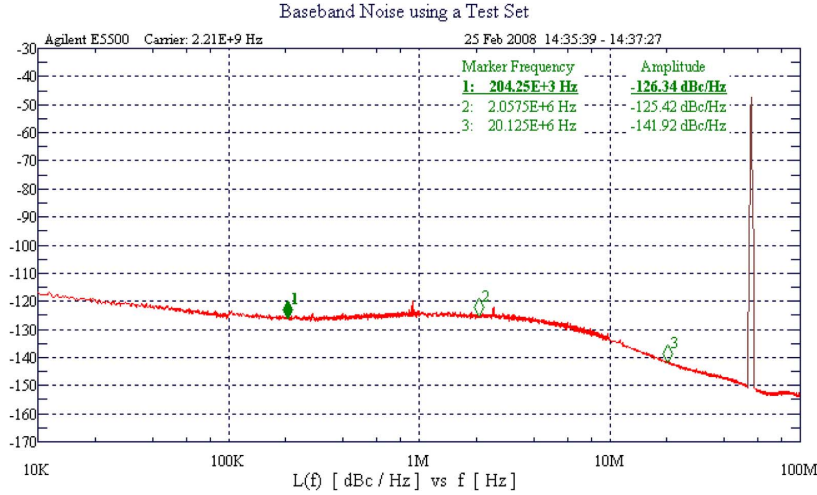


Fig. 14. Measured PLL output phase noise.

Switching on/off the FLL has negligible effect on the spectrum. The PLL output rms jitter can be related to the phase noise as

$$\sigma_t^2 = \frac{2 \times \int_{f_l}^{f_h} \mathcal{L}(f) df}{(2\pi f_{\text{out}})^2} \quad (21)$$

where  $[f_l, f_h]$  is the integration region. Integrating the phase noise spectrum from 10 kHz to 40 MHz yields a total phase noise of  $-56.8$  dBc, which translates to an rms jitter of 0.15 ps at the 2.21 GHz output frequency.

According to the noise summary in Spectre RF PNoise simulations, the inverter chain Ref buffer, the crystal oscillator and the rest circuits contributes 50%, 20%, and 30% to the in-band phase noise at 200 kHz, respectively. The Ref buffer noise is dominated by the first inverter in the chain as its input is a slow 55.25 MHz sine-wave. The in-band phase noise due to this inverter can be related to the voltage noise  $v_{\text{out},n}^2$  and slew-rate  $SR_{\text{out}}$  at its output crossing moment as [10]

$$\begin{aligned} \mathcal{L}_{\text{in-band,Ref-Buffer}} &\approx \frac{1}{2} \cdot N^2 \cdot S_{\phi,\text{Ref-Buffer},n} \\ &= 4\pi^2 \cdot N^2 \cdot f_{\text{ref}} \cdot \frac{v_{\text{out},n}^2}{SR_{\text{out}}^2}. \end{aligned} \quad (22)$$

Since the input of the inverter is a slow sine-wave Ref,  $SR_{\text{out}}$  can be calculated as the voltage gain  $G_v$  times the Ref slew-rate:<sup>2</sup>

$$\mathcal{L}_{\text{in-band,Ref-Buffer}} = 4\pi^2 \cdot N^2 \cdot f_{\text{ref}} \cdot \frac{v_{\text{out},n}^2}{(G_v \cdot A_{\text{ref}} \cdot 2\pi f_{\text{ref}})^2} \quad (23)$$

with  $A_{\text{ref}}$  the Ref amplitude. Therefore, the in-band phase noise due to Ref buffer will be higher with a smaller  $A_{\text{ref}}$ . The measured in-band phase noise at 200 kHz offset with different

<sup>2</sup>In order to achieve lower phase noise, we could use a higher  $f_{\text{ref}}$  or steepen the Ref clock edges before it is fed to the chip. However, this is not done as it only shifts the problem to other blocks, e.g., to the generation of a clean high frequency Ref. When the Ref slew rate is very high, e.g.,  $f_{\text{ref}}$  is very high or Ref is a square wave instead of a sine-wave,  $SR_{\text{out}}$  will be eventually limited by I/C at the inverter output.

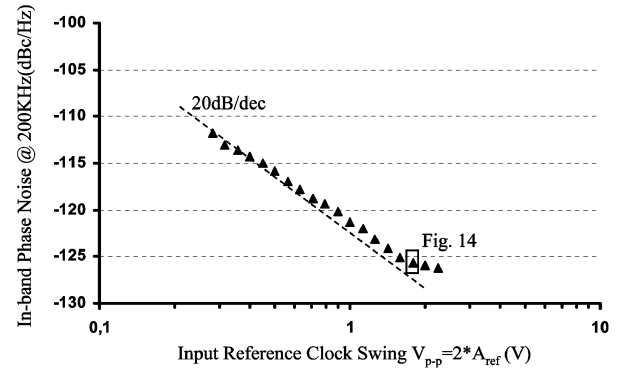


Fig. 15. Measured in-band phase noise at 200-kHz offset with different input reference clock amplitude.

$A_{\text{ref}}$  is shown in Fig. 15. The phase noise is indeed higher with a smaller  $A_{\text{ref}}$ , in a 20 dB/dec manner as predicted by (23). This also fits to the expectation that the Ref buffer is the dominant source of the in-band phase noise.

The PLL reference spur was measured with an Agilent Spectrum Analyzer E4440A to be  $-46$  dBc at 55.25 MHz offset as shown in Fig. 16. It is caused by insufficient isolation between the VCO and the sampler, and can be improved in a redesign.

Table I summarizes the PLL performance and shows a comparison with a few previously published low noise PLLs. When directly compared, the in-band phase noise achieved in this work is at least 18 dB lower. However, this direct comparison is unfair since the classical PLL in-band phase noise level is systematically dependent<sup>3</sup> on the choice of  $N$  and  $f_{\text{ref}}$ . The often used normalized in-band phase noise which normalizes this systematic dependency out is defined as [20]

$$\mathcal{L}_{\text{norm}} = \mathcal{L}_{\text{in-band}} - 20 \log N - 10 \log f_{\text{ref}}. \quad (24)$$

After normalization, the in-band phase noise of this design is at least 13 dB lower than previous designs. Note that this is achieved together with several times less power as well as active area.

<sup>3</sup>In the SSPLL, the PD/CP noise is not related to  $N$ . However, the Ref buffer noise, which dominates the in-band phase noise, is still multiplied by  $N^2$  as in a classical PLL.

TABLE I  
PLL PERFORMANCE AND COMPARISON

	This Work	[9] <sup>*</sup>	[7]	[6]	[5]	[3]
Output Freq. (GHz)	2.21	3.67	20	3.125	2.4	10
Reference Freq. (MHz)	55.25	50	78	62.5	25	2500
In-band Phase Noise	-126@200kHz	-108@400kHz	-81@60kHz	-108@100kHz	-108@1MHz	-109@600kHz
Normalized In-band Phase Noise (dBc/Hz <sup>2</sup> )	-235@200kHz	-222@400kHz	-207@60kHz	-220@100kHz	-218@1MHz	-215@600kHz
Power (mW)	7.6	39	22.5	25	19.5	81
RMS Jitter (ps)	0.15 (10k-40M)	0.2 (1k-40M)	?	0.56 (1k-50M)	0.6 (10k-40M)	0.22 (10k-20M)
Active Area (mm <sup>2</sup> )	0.18	0.95	0.6	0.43	0.70	0.71
Technology (μm)	0.18	0.13	0.13	0.13	0.12	0.18

\* It is a fractional-N PLL

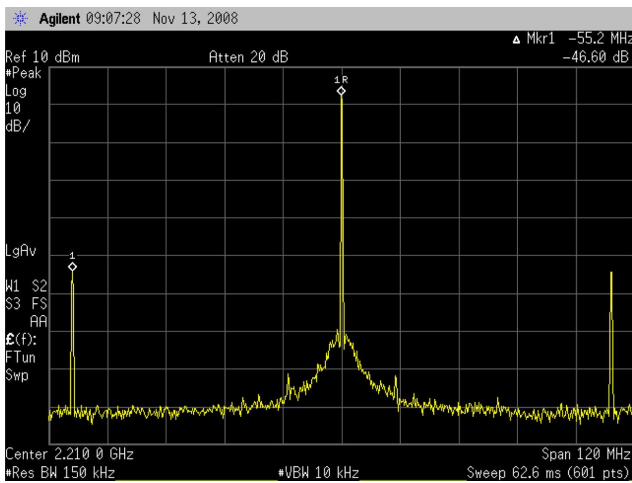


Fig. 16. Measured PLL output spectrum.

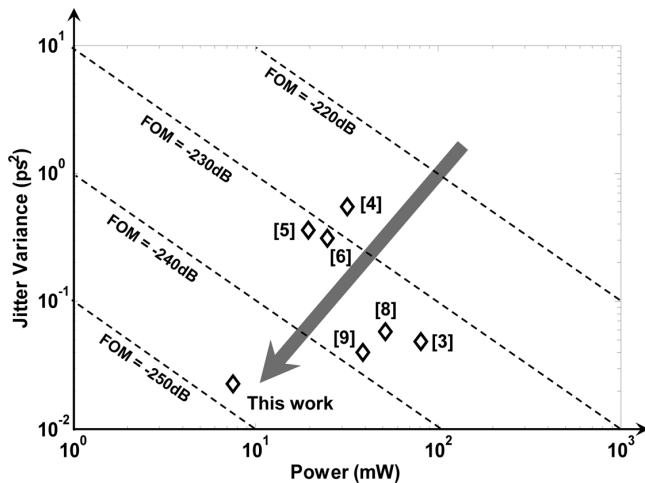


Fig. 17. Jitter and power comparison between this work and the classical PLLs.

For the PLL as a whole, it can be shown that the PLL jitter performance is to a large degree systematically related to its power consumption. In order to take the tradeoff between jitter and power into account and make a fair comparison, a benchmarking figure-of-merit (FOM) for low jitter PLL designs can be defined as [10]

$$\text{FOM} = 20 \log \frac{\sigma_t}{1 \text{ s}} + 10 \log \frac{P}{1 \text{ mW}}. \quad (25)$$

Fig. 17 shows the jitter and power performance of this work and a few representative classical PLLs. This work achieves the lowest jitter as well as lowest power and thus has the best PLL FOM.

## VI. CONCLUSION

Design considerations and measurement results of a fully integrated 2.21-GHz PLL in a standard 0.18-μm CMOS process with reduced in-band phase noise have been presented. This PLL employs a PD/CP that sub-samples a high frequency VCO output with a low frequency reference clock. In contrast to what happens in a classical PLL, the PD/CP noise is not multiplied by  $N^2$  in this sub-sampling PLL, resulting in a low noise contribution from the PD/CP. Moreover, no frequency divider is needed in the locked state thus divider noise and power are eliminated. Despite of the low noise feature, a sub-sampling PLL has drawbacks like difficulty of integration (large filter capacitor needed due to high detection gain) and limited frequency acquisition range. In order to overcome these drawbacks, pulsewidth gain control is added to the sub-sampling PD/CP to reduce the detection gain and thus the needed filter capacitor value. A classical three-state PFD/CP based PLL with a dedicated dead zone is added as a frequency locked loop which guarantees correct frequency locking without degenerating jitter performance. Operating at 1.8 V with a 55.25 MHz sine wave reference clock, the 2.21 GHz PLL consumes 4.2 mA. The measured in-band phase noise is -126 dBc/Hz at 200 kHz offset and the rms output jitter integrated from 10 kHz to 40 MHz is 0.15 ps.

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analog circuits in general and more specific in PLLs and DLLs.

**Xiang Gao** (S'07) was born in Zhejiang Province, China, in 1983. He received the B.E. degree (*with honor*) from the Zhejiang University, Hangzhou, China, in 2004 and the M.Sc. degree (*cum laude*) from the University of Twente, Enschede, the Netherlands, in 2006, both in electrical engineering. He is currently working towards the Ph.D. degree in the IC Design group of the University of Twente.

During summer 2007 and summer 2008, he was a visiting scholar in NS Labs, National Semiconductor, Santa Clara, CA. His research interests are RF and



**Eric A. M. Klumperink** (M'98–SM'06) was born on April 4, 1960, in Lichtenvoorde, The Netherlands. He received the B.Sc. degree from HTS, Enschede, The Netherlands, in 1982. After a short period in industry, he joined the Faculty of Electrical Engineering of the University of Twente (UT) in Enschede in 1984, participating in analog CMOS circuit design and research. This resulted in several publications and a Ph.D. thesis, in 1997 ("Transconductance based CMOS circuits").

After receiving his Ph.D., he started working on RF CMOS circuits. He is currently an Associate Professor at the IC-Design Laboratory which participates in the CTIT Research Institute (UT). He holds several patents and has authored or coauthored more than 80 journal and conference papers.

In 2006 and 2007, Dr. Klumperink served as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, and since 2008 for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I. He was a co-recipient of the ISSCC 2002 Van Vessel Outstanding Paper Award.



**Mounir Bohsali** (S'01) was born on March 21, 1980, in Beirut, Lebanon. He received the B.S. degree in computer engineering from North Carolina State University, Raleigh, in 2001, and the M.S. and Ph.D. degree in electrical engineering from the University of California at Berkeley in 2004 and 2008, respectively.

He is currently with National Semiconductor, Santa Clara, CA. His research interests include the design of microwave CMOS power amplifiers and modeling of microwave passive structures as well as

the design of low noise PLLs.



**Bram Nauta** (M'91–SM'03–F'08) was born in Hengelo, The Netherlands, in 1964. In 1987 he received the M.Sc. degree (*cum laude*) in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies.

In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, The Netherlands, where he worked on high speed AD converters and analog key modules. In 1998 he returned to the University of Twente, as full Professor heading the IC Design group, which is part of the CTIT Research Institute. His current research interest is high-speed analog CMOS circuits. He is also part-time consultant in industry and in 2001 he co-founded Chip Design Works. His Ph.D. thesis was published as a book: *Analog CMOS Filters for Very High Frequencies* (Springer, 1993), and he received the Shell Study Tour Award for his Ph.D. work.

From 1997 until 1999 he served as Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART II-ANALOG AND DIGITAL SIGNAL PROCESSING. After this, he served as Guest Editor, Associate Editor (2001–2006), and from 2007 as Editor-in-Chief for the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He is also member of the technical program committees of the IEEE International Solid State Circuits Conference (ISSCC), the European Solid State Circuit Conference (ESSCIRC), and the Symposium on VLSI Circuits. He was a co-recipient of the ISSCC 2002 Van Vessel Outstanding Paper Award, and an elected member of IEEE SSCS AdCom.